CBCS SCHEME

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18CS34

Third Semester B.E. Degree Examination, July/August 2021
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions.*

1 a. With neat block diagram, explain the basic operational concepts of a computer. **(05 Marks)**

b. Write basic performance equation and explain and define the terms involved in it. **(05 Marks)**

c. What is an Addressing mode? Explain the following addressing modes with one example for each : i) Absolute ii) Immediate iii) Indirect iv) Auto increment. **(10 Marks)**

2 a. Explain Big – Endian and Little – Endian assignment. Consider a computer that has a byte addressable memory organized in 32 words, according to Little – Endian scheme. A program reads ASCII characters entered at a keyboard and store them in successive byte location starting at 2000. Show how the contents of the three memory words at locations 2000, 2004 and 2008 after the string "VTU BELAGAVI" has been entered. (ASCII codes : V = 56H , T = 54H , U = 55H , " " = 20H , B = 42H , E = 45H , L = 4 CH , A = 41H , G = 47H , I = 49H). **(05 Marks)**

b. Register R_1 and R_2 of computer contain the decimal values 1200 and 4600. What is Effective Address (EA) of the memory operand in each of the following instructions?
i) Load 20 (R_1), R_5 ii) Move # 3000 , R_5 iii) Store 30 (R_1, R_2) , R_5
iv) Add – (R_2) , R_5 v) Subtract (R_1) + , R_5. **(05 Marks)**

c. Explain Logical shift and Rotate instructions with examples. **(10 Marks)**

3 a. Explain Memory mapped I/O and I/O mapped I/O. **(06 Marks)**

b. With neat diagram, explain Centralized bus arbitration and distributed bus arbitration. **(08 Marks)**

c. What is DMA? Explain the registers in a DMA interface. **(06 Marks)**

4 a. Define Interrupt. With example, explain the concept of interrupt. What are the overheads incurred in handling interrupt? **(06 Marks)**

b. With neat diagram, explain the synchronous bus transfer during an input operation. **(08 Marks)**

c. Explain the tree structure of USB with split bus operation. **(06 Marks)**

5 a. Define i) Memory latency ii) Memory Bandwidth iii) Hit – rate iv) Miss penalty. **(04 Marks)**

b. With a neat diagram, explain the internal organisation of a 2M × 8 dynamic memory chip. **(10 Marks)**

c. With a neat diagram, explain the memory hierarchy with respect to speed, size and cost. **(06 Marks)**

6 a. With neat diagrams, explain internal structure of i) Static RAM, cell and ii) ROM cell. **(08 Marks)**

b. What is Memory Mapping? With neat diagram explain
i) Direct mapping ii) Set Associative mapping. **(12 Marks)**

7 a. Perform following operations on the 5 – bit signed numbers using 2's complement representation system. Also indicate whether the overflow has occurred.
i) (-9) + (-7) ii) (+7) – (-8). **(04 Marks)**

b. With neat diagram, explain 4 – bit carry – look ahead adder. **(08 Marks)**

c. Perform multiplication for -13 and + 9. Using Booth's Algorithm. **(08 Marks)**

8 a. Design a logic circuit to perform addition / subtraction of two 'n' bit numbers X and Y. **(04 Marks)**

b. Perform the division of numbers 8 by 3 (8÷3) using Restoration Division method. **(08 Marks)**

c. With neat diagram, explain Register configuration for sequential multiplication. **(08 Marks)**

9 a. With a neat diagram, explain Single bus organisation of data path inside a processor. **(10 Marks)**

b. What are the actions required to Excuse a complete instruction. Add (R_3) , R_1. Give the control sequence for execution of instruction Add (R_3), R_1. **(10 Marks)**

10 a. With neat diagram, explain the Microprogrammed Control method for design of control unit and write the micro – routine for the instruction Branch < 0. **(10 Marks)**

b. Bring out the difference between Microprogrammed control and Hard – wired control. **(04 Marks)**

c. With neat diagram, explain 4 – Stage pipeline. **(06 Marks)**

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